IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please amend the title as follows:

~~**USING STABILIZERS IN ELECTROLESS SOLUTIONS TO INHIBIT PLATING OF FUSES**~~
INTERMEDIATE SEMICONDUCTOR DEVICE STRUCTURE

IN THE SPECIFICATION:

Please amend paragraph **[0001]** as follows:

[0001] This application is a divisional of application Serial No. 10/154,755, filed May 24, 2002, ~~pending.~~ now U.S. No. Patent 6,709,980, issued March 23, 2004.

Please amend paragraph **[0003]** as follows:

[0003] State of the ~~Art.~~ Art: Fuses or fusible links are commonly used to connect electrical components on the surface of a semiconductor device with conductive traces to form circuit assemblies. Fuses are also used to provide a level of redundancy in the semiconductor device. For example, if a defective portion of the semiconductor device is found during testing or probe, the fuse connecting that portion is opened or blown, making that portion nonfunctional. However, since the semiconductor device is fabricated with many portions that perform the same function, the semiconductor device still functions after the fuse is opened. By building redundancies into semiconductor devices, manufacturers can increase their yields because devices that otherwise would be defective can still be used.

Please amend paragraph **[0004]** as follows:

[0004] In intermediate structures of certain semiconductor devices, such as static random access memory ("SRAM") and ~~FLASH~~ Flash memory chips, fuses are exposed at the wafer level. The fuses are typically formed from conductive materials such as metals or polysilicon. The fuse is opened, or "blown," by exposure to a laser beam or electrical current, which causes the metal or polysilicon to rapidly heat up and vaporize. This vaporized material is scattered and deposited across areas of the intermediate structure. In addition to causing shorts, the vaporized material may be undesirably deposited on the blown ends of the opened fuse, thereby reforming the two ends. The ends of the opened fuse may also be reformed if metal features are formed on the intermediate structure after the fuse has been opened. For example, metal of the metal feature may reform the fuse by spanning between the two, opened ends. Since the formation of metal features is necessary to electrically connect the semiconductor device, reformation of fuses opened during probe testing is problematic.

Please amend paragraph **[0014]** as follows:

[0014] The intermediate structure may be an intermediate structure of an SRAM or ~~FLASH~~ Flash memory chip that comprises at least one bond pad and at least one opened fuse. The metal feature is electrolessly plated onto the at least one bond pad, without reforming the opened fuse, by adjusting the concentration of stabilizer.

Please amend paragraph **[0022]** as follows:

[0022] The intermediate structure of the semiconductor device may comprise a first exposed metal structure and a second exposed metal structure. The first exposed metal structure may be an exposed metal structure present on the surface of the intermediate structure and may be the surface upon which formation of the metal feature occurs. The second exposed metal structure may be a smaller structure upon which formation of the metal feature is not desired. In one exemplary embodiment, discussed herein, the first exposed metal structure is a metal bond pad, or interconnect pad, and the second exposed metal structure is an opened fuse. The bond pad may be rectangular and have dimensions of 40-80 μm by 40-80 μm. In this embodiment, the intermediate structure of the semiconductor device comprises an intermediate structure of a memory chip, such as an SRAM or ~~FLASH~~ Flash memory, wherein fuses are exposed at the wafer level.

Please amend paragraph **[0031]** as follows:

[0031] In an exemplary embodiment, an intermediate structure of an SRAM or ~~FLASH~~ Flash memory chip is provided. The intermediate structure comprises at least one bond pad as the first exposed metal structure, such as at least one copper bond pad, which is deposited by electroplating or other techniques known in the art. The intermediate structure also comprises at least one fuse as the second exposed metal structure. The at least one fuse is exposed at the wafer level and is preferably metallic. However, the fuse may also comprise polysilicon. The intermediate structure is probe tested for defects and defective regions are rendered nonfunctional by opening the fuses to those defective regions. Preferably, the intermediate structure comprises

at least one opened fuse. After the fuse has been opened, the interconnect cap is formed over the at least one copper bond pad to improve bonding thereto. To form the interconnect cap, the at least one copper bond pad is first immersion plated with palladium. Then, a layer of nickel is electrolessly plated over the palladium, followed by immersion plating of a layer of gold to prevent the nickel layer from oxidizing.

Please amend paragraph **[0032]** as follows:

[0032] To electrolessly plate the nickel, the intermediate structure of the SRAM or ~~FLASH~~ Flash memory chip is placed in an EN plating solution, such as ConPac 2.0, available from Pac Tech (Nauen, Germany). The nickel is plated in a layer approximately 3-5 μm thick. Other EN plating solutions that plate nickel at an appropriate thickness for use in an interconnect cap may also be used.

Please amend paragraph **[0035]** as follows:

[0035] The semiconductor wafer 2 comprising the plurality of opened fuses 6′ is placed in a solution of ConPac 2.0. After allowing the plating reaction to proceed for an appropriate amount of time, the bond pads 4 and fuses 6 are examined by SEM to determine whether the nickel is selectively plated onto the bond pads 4. For each size of bond pad 4, the amount of nickel plated on the bond pads 4 is compared to the amount formed on the opened ~~fuses.~~ fuses 6′. Bond pads 4 larger than approximately 5 μm have a layer of nickel plated on them without nickel forming on the opened ~~fuses.~~ fuses 6′.